Real-Time JPEG Compression

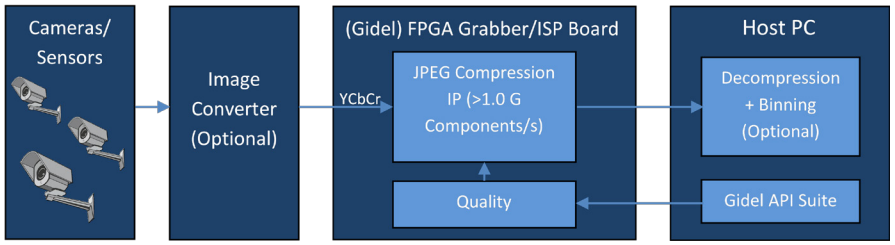
For High-Performance Camera Streams

Key Features

- Real-time JPEG compression of high performance sensor image streams
- IP for FPGA based frame grabbers
- Compression performance beyond 1 Giga components/s
- Architectural design enabling significant performance enhancement
- Support for 422, 444 and 420 color subsampling encoding
- For 422 sampling, throughput beyond 500 MPixels/s
- Ultra-compact IP
- Low latency
- Selectable JPEG compression quality
- Host interface with API suite for software control
- Support for virtually unlimited image width using minimal memory resources
- Supported by Gidel's reconfigurable acquisition flow enabling adding compression and ISP blocks
- Supported by Gidel's InfiniVision IP for acquisition from multi-cameras/sensors
- Supported by the Gidel's Dev Kit for highly efficient development on FPGA
- Optional binning decompression software
- Option for software model for compression simulations

Target Applications

- Recording Systems
- Broadcasting and Video
- Smart Cities and Surveillance
- Autonomous Cars
- Embedded Vision



The Gidel JPEG compression (encoder) IP, gil_jpeg_encode, enables high-performance JPEG compression on FPGA. The compression IP is unique in its fast processing capacity, low latency and compact silicon utilization. As a result of its compactness, the IP can be implemented on a small FPGA device to compress high-performance camera image streams or, alternatively, the IP can be instantiated multiple times on a single larger FPGA device. The IP includes a host interface and an API suite for software control.

The JPEG IP's input stream is in YCbCr format with an optional converter from RGB, monochrome, etc. The degree of compression can be adusted allowing selectable tradeoff between storage size and image quality. Color subsampling can be encoded in 4:2:2, 4:4:4 or 4:2:0 formats. The following table shows a compression performance example using 4:2:2 encoding at 540 MPixels/s. The latency for this example is 130 uS.

FPGA	Throughput	Line size	Bit/ component	Area (ALMs)	M20K	DSP blocks
Arria 10 (slowest device)	1,080 Mega components/s	8K pixels/line	8	5000	151	64

Compression Performance Example

The IP is supported by Gidel's comprehensive ecosystem allowing tailoring optimized solutions that may include image processing, vision algorithms and a concurrent recording system. Recording system may also be complemented by Gidel's CamSim playback system.

The IP is also supported by optional software for image binning decompression. This feature, for example, can be used for displaying videos from multi-cameras during a recording session or for quickly reviewing a large image set.

Gidel's Supporting Ecosystem

The Gidel ecosystem includes infrastructure and development tools enabling to quickly develop a high-end custom FPGA frame grabber with real-time compression and image processing capabilities. The ecosystem includes:

- ***FPGA Frame Grabber and Image Processing Systems***

Gidel offers FPGA-based systems with open reconfigurable acquisition flow allowing the user to customize the grabbing and to add user image processing blocks including the JPEG compression IP. The frame grabber boards interface with the host computer via PCIe or alternatively may operate as a standalone system.

- ***FPGA Multi-Camera Acquisition System***

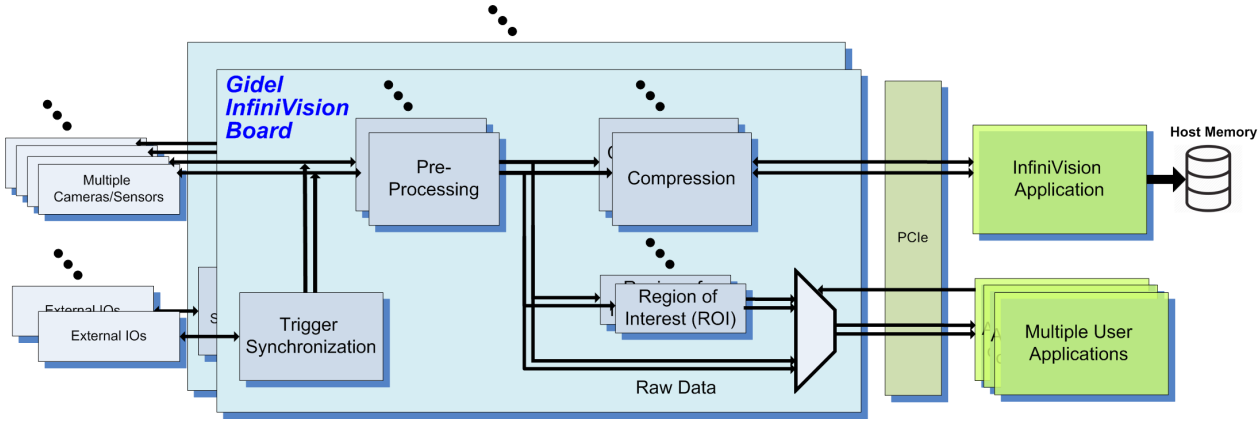
The Gidel InfiniVision is a unique image acquisition system designed for grabbing from multi-cameras/sensors. Combined with real-time compression as much as 100 camera video streams can be supported simultaneously.

- ***Highly Efficient Video Recording & Playback Systems***

Based on real-time compression, Gidel offers a recording system that is exceptionally efficient in both its offloading throughput and compactness of required memory resources. This capability has significant benefits for applications with demanding bandwidth and/or memory resources, e.g., field applications. Based on Gidel's CamSim a playback sub-system, images can then be retrieved at the original throughput for a variety of application tasks.

- ***Proc Developer's Kit***

The Proc Developer's tools enable to map the FPGA board to the desired data flow and interfaces. The following figure demonstrates one possible implementation using InfiniVision, compression and custom image processing.



- ***Gidel Customization Services***

Based on 25 year experience, Gidel offers customization services for developing tailored Vision/Imaging systems according to the customer's specifications. Gidel takes advantage of its uniquely flexible and powerful infrastructure to quickly implement the target application within impressive short time spans.

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